

# register management flip-flops

inputis 1

reg1last

reg1full

# data buffer registers

reg 1

outputis 1

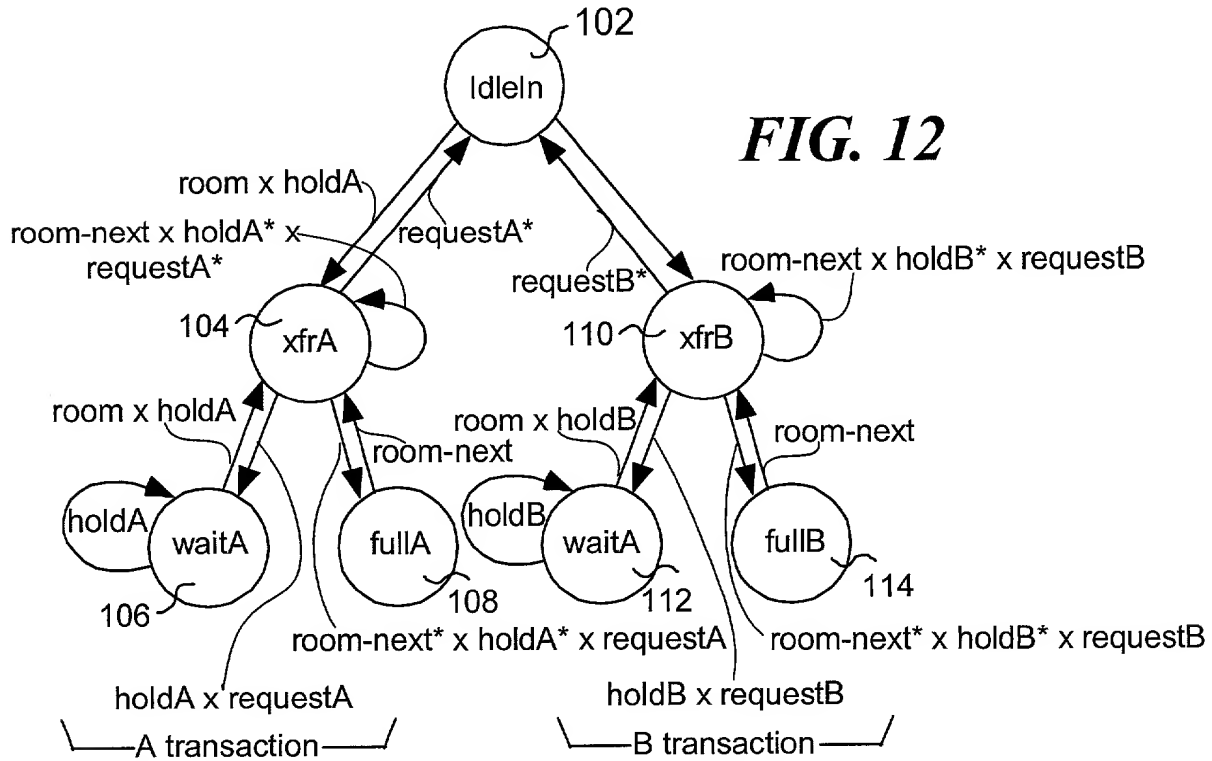
reg2last

reg2full

reg 2

**FIG. 11**

**FIG. 12**



transaction = IdleIn\*

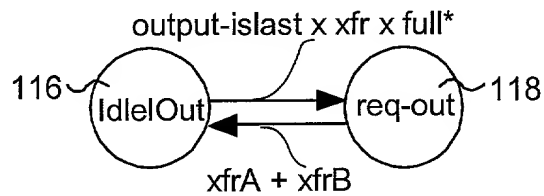
room-next = empty + xfr

room = reg1full\* + reg2full + xfr

full = reg1full x reg2full

empty = reg1full\* x reg2full\*

**FIG. 13**



register management flip-flops

inputis 1

route2A1

reg1last

reg1full

data buffer registers

reg 1

outputis 1

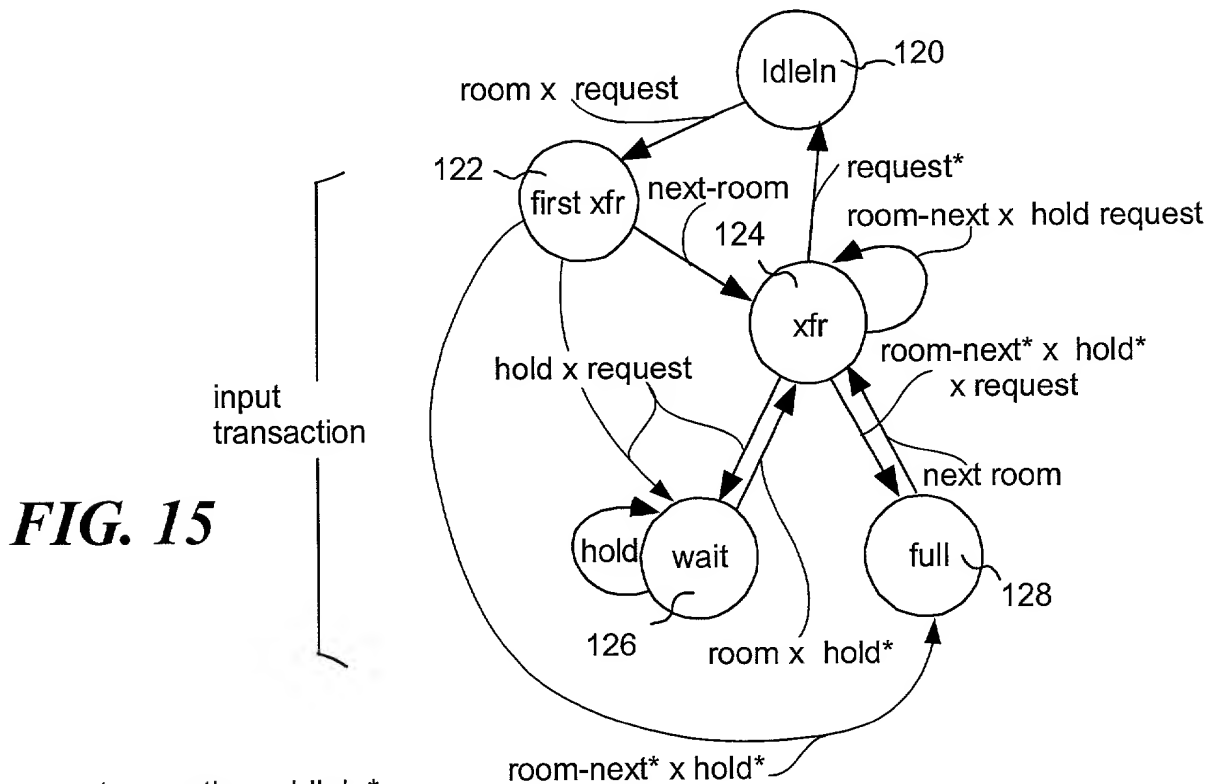
route2A2

reg2last

reg2full

reg 2

**FIG. 14**



transaction = IdleIn\*

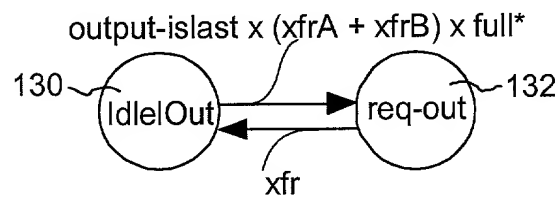
room-next = empty + xfrA + xfrB

room = reg1full\* + reg2full\* + xfrA + xfrB

full = reg1full x reg2full

empty = reg1full\* x reg2full\*

**FIG. 16**



# register management flip-flops

inputs 1

reg1last

reg1full

# data buffer registers

reg 1

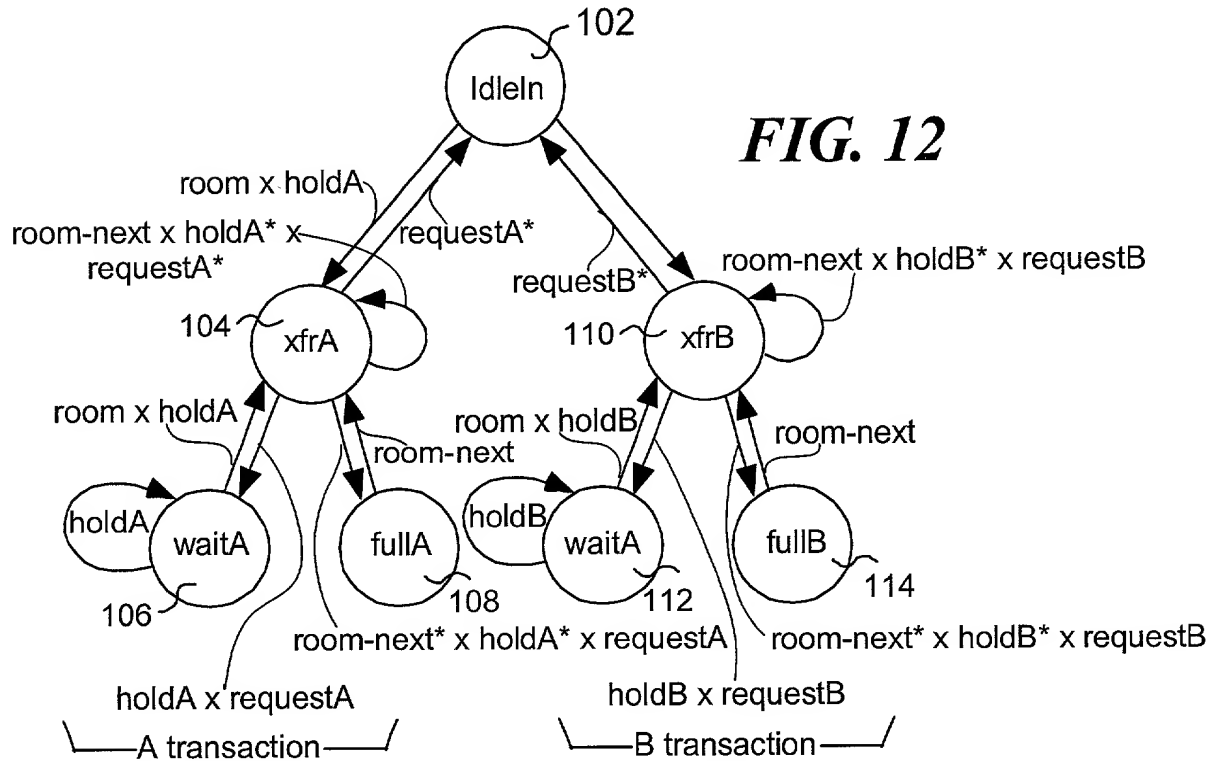
outputs 1

reg2last

reg2full

reg 2

FIG. 11



transaction = IdleIn\*

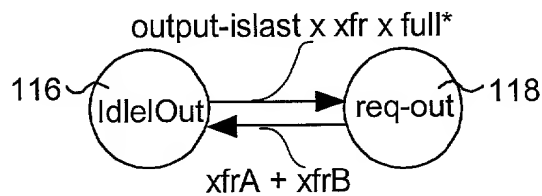
room-next = empty + xfr

room = reg1full\* + reg2full + xfr

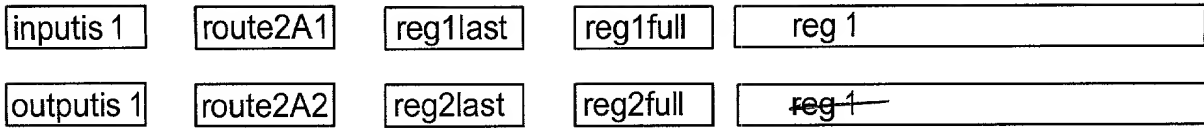
full = reg1full x reg2full

empty = reg1full\* x reg2full\*

FIG. 13

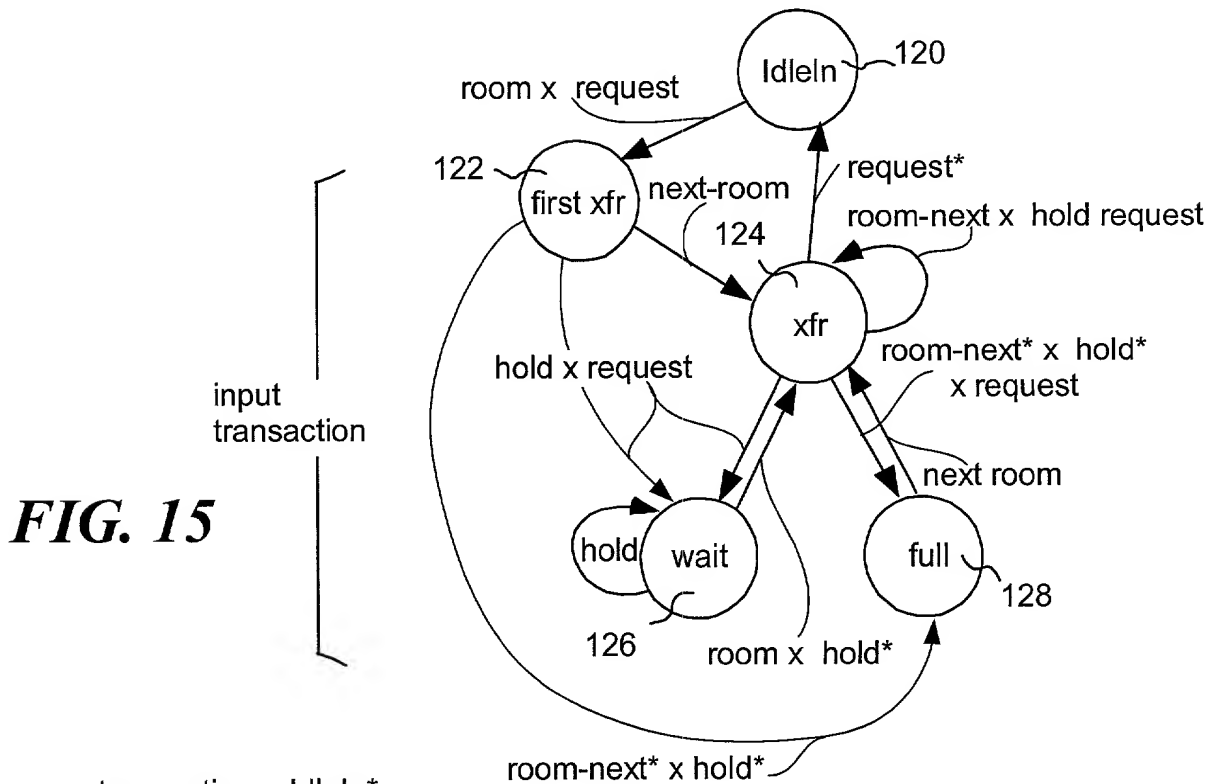


register management flip-flops



reg 2

**FIG. 14**



transaction = IdleIn\*

room-next = empty + xfrA + xfrB

room = reg1full\* + reg2full\* + xfrA + xfrB

full = reg1full x reg2full

empty = reg1full\* x reg2full\*

